This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

Claim 1 - 8 (canceled)

Claim 9 (original): A flip chip package, comprising

an integrated circuit chip having interconnect bumps formed on input/output pads in a specified arrangement in a surface thereof, and a package substrate having a plurality of bond pads in a complementary arrangement in a subjacent surface of the package substrate, wherein

second level interconnect sites are arranged in a second surface of the package substrate, and second level interconnect structures are connected to the respective second level interconnect sites, and wherein

a fill volume is defined between the integrated circuit chip and the package substrate, the fill volume being at least partly filled with at least one fill material, each said fill material having a selected specific elastic modulus, wherein regions of the fill volume that overlie the second level interconnect sites contain a lower specific elastic modulus fill material.

Claim 10 (original): The flip chip package of claim 9 wherein the fill volume includes a first fill zone comprising a plurality of generally columnar volumes, generally overlying the plurality of second level interconnect sites; and the second fill zone consists of the remainder of the fill volume.

Claim 11 (original): The flip chip package of claim 10 wherein at least a part of the first fill zone contains a first material having a lower specific elastic modulus, and at least a part of the second fill zone contains a second material having a higher specific elastic modulus.

Claim 12 (original): The flip chip package of claim 11 wherein the first fill material has a specific elastic modulus less than about 0.5 GPa.

Claim 13 (original): The flip chip package of claim 11 wherein the second fill material has a specific elastic modulus greater than about 5 GPa.

Claim 14 (original): The flip chip package of claim 13 wherein the second fill material has a specific elastic modulus in a range about 5 GPa to about 15 GPa.

Claim 15 (original): The flip chip package of claim 11 wherein the second fill material comprises an epoxy.

Claim 16 (original): The flip chip package of claim 15 wherein the second fill material comprises an anhydride curable epoxy.

Claim 17 (original): The flip chip package of claim 11 wherein the first fill zone comprises voids in the fill material within the fill volume.

Claim 18 (original): The flip chip package of claim 11 wherein the first fill material comprises an adhesive.

Claim 19 (original): The flip chip package of claim 18 wherein the first fill material comprises a silicon adhesive.

Claim 20 (original): A method for making a flip chip package configured for interconnection to a printed circuit board, comprising

providing an integrated circuit chip having a surface;

providing a package substrate having a first surface and a second surface, the second surface being provided with a plurality of second level interconnect sites, the locations of the second level interconnect sites defining a plurality of first fill zone areas over the first surface of the package substrate, the remainder of the first surface of the package substrate constituting a second fill zone area;

dispensing at least a second fill material, having a specific elastic modulus greater than about 5 GPa, within the second fill zone area on the first surface of the package substrate; and

assembling the integrated circuit chip and the package substrate so that the second fill material is confined in a second fill zone within a volume defined between the integrated circuit chip surface and the first surface of the package substrate.

Claim 21 (original): The method of claim 20 wherein the second fill material has a specific elastic modulus in a range about 5 GPa to about 15 GPa.

Claim 22 (original): The method of claim 20, further comprising, prior to assembling the package, dispensing a first fill material having a specific elastic modulus less than about 0.5 GPa within the first fill zone area on the first surface of the package substrate.